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CMPT220 Midterm Examination
March 12, 2002
Closed Book, 1 Letter Size sheet of notes allowed
Answer all questions on this examination paper
75 MARKS

1. *(4 marks)* When implementing logic functions using CMOS technology, what is the purpose of the pull-up network? The pull-down network?

The pull-up network must be able to attain V_{DD} when necessary and the pull-down network must be the opposite of the pull-up network and must get V_0 when necessary.
The PUN is also made up of PMOS transistors while the PDN is made up of NMOS transistors.

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2. *(4 marks)* What is the major problem associated with rapidly performing addition or subtraction with larger numbers? What was the solution?

The problem is the loss of precision in the lower-end bits.

0

3. *(4 marks)* What is "high-impedance" and why is it important?

High-impedance is a state in a wire usually represented as Z and it is important because it doesn't matter if the output is a 1 or a 0 and it helps solve the fan-out problem.

1

4. *(4 marks)* What are two uses for a multiplexer?

One use is to determine which inputs should go on in a circuit depending on what the control signals are set at.
Another use is to determine what value to return from a look-up table.

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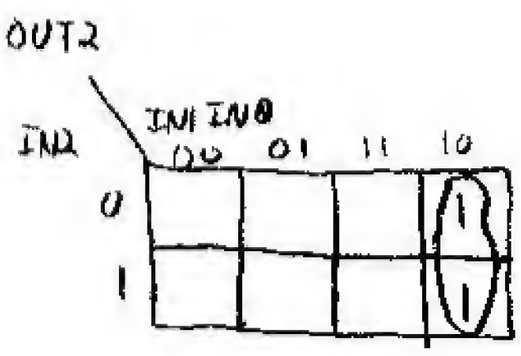
5. *(10 marks)* Given the following table of inputs versus outputs for a logic circuit, answer the following questions using variables of the form INx and OUTx to denote the x^{th} bit and where x = 0 represents the lowest order bit.

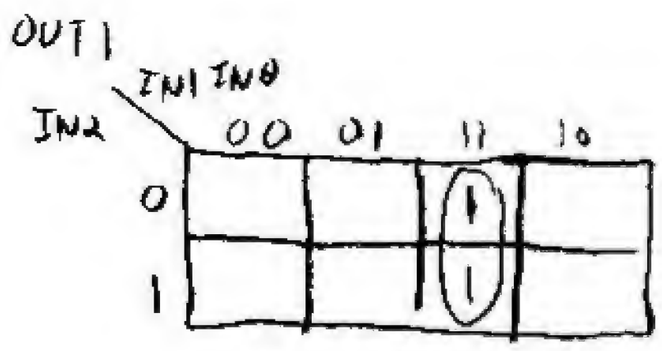
Input	0	1	3	2	6	7	5	4
Output	0	1	2	4	4	2	1	0

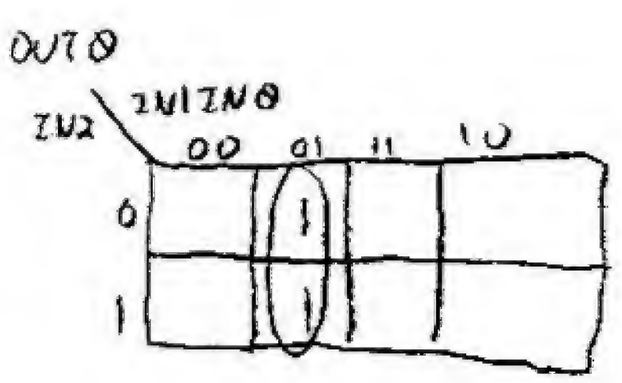
a) Draw the Karnaugh Maps for each output bit, clearly identifying the inputs and outputs.
b) Minimize each K-Map using SOP form and clearly identify your solution. **Please do not attempt to optimize your solution beyond the K-Map derivation!**

IN2	IN1	IN0	OUT2	OUT1	OUT0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	1	0

a)







b) $OUT2 = IN1\,\overline{IN0}$ $OUT1 = IN1\,IN0$ $OUT0 = \overline{IN1}\,IN0$

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6. *(10 marks)* Write the Entity and Architecture VHDL code for the logic function
$F(x2, x1, x0) = \Sigma m(1, 2, 4, 7)$

```
LIBRARY ieee;
USE ieee_std_logic_1164.all;

ENTITY testquestion IS
        PORT (x2, x1, x0 : IN BIT;
              F          : OUT BIT);
END testquestion

ARCHITECTURE LogicFunc OF testquestion IS
BEGIN
        F <= (x2 AND NOT x1) AND NOT x0) OR (NOT x2 AND NOT x1 AND x0) OR
             (x2 AND x1 AND x0) OR (NOT x2 AND x1 AND NOT x0);
END LogicFunc;
```

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7. *(8 marks)* Express the following K-maps as logic functions of the required form.

a) F(x4, x3, x2, x1) = $\overline{x3}\,\overline{x2}\,\overline{x1} + x4\,\overline{x3}\,\overline{x1} + x3\,\overline{x2}\,x1 + x4\,x3\,x1 + \overline{x4}\,x3\,x2\,\overline{x1}$ Sum of Products Form

F

x4x3 \ x2x1	00	01	11	10
00	1	0	0	0
01	0	1	0	1
11	0	1	1	0
10	1	0	0	1

b) G(x1, x2, x3, x4) = $(x2 + x4)(x1 + \overline{x3})(\overline{x2} + \overline{x4})$ Product of Sums Form

G

x1x2 \ x3x4	00	01	11	10
00	0	1	1	0
01	0	D	D	0
11	1	0	0	1
10	0	1	1	0

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8. *(4 marks)* What is the difference between a binary encoder and a binary decoder?

A binary decoder has n inputs and produces 2^n outputs which are one-hot encoded or only one of the outputs is 1. A binary encoder has 2^n inputs which are one-hot encoded and produces n outputs.

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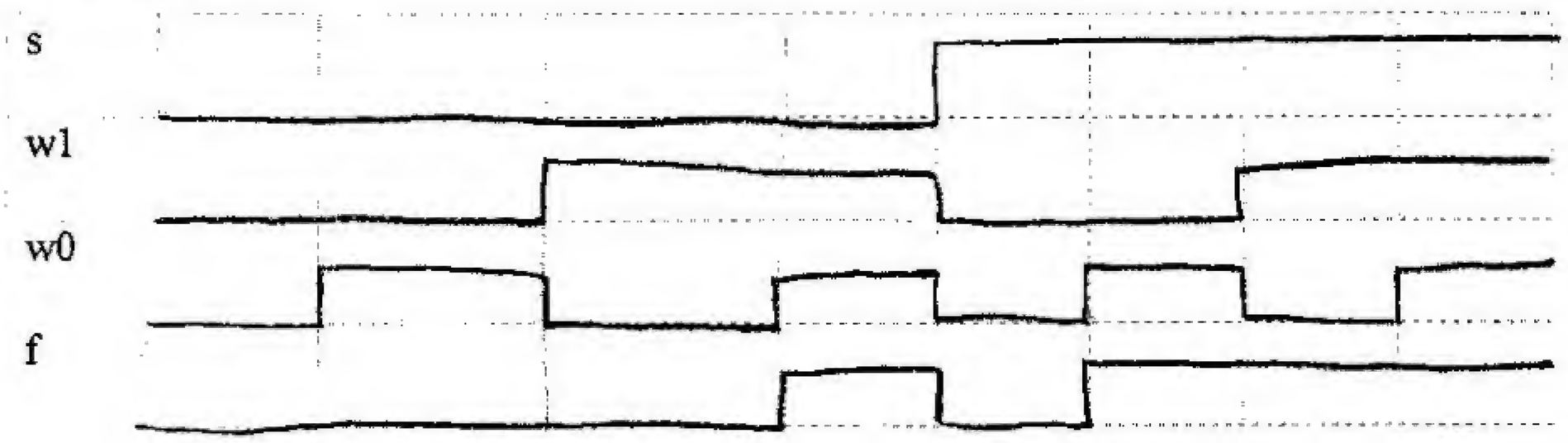
9. *(8 marks)* Given the following VHDL code, draw the timing diagram for the resulting circuit as if you were the Max+plus II development environment.

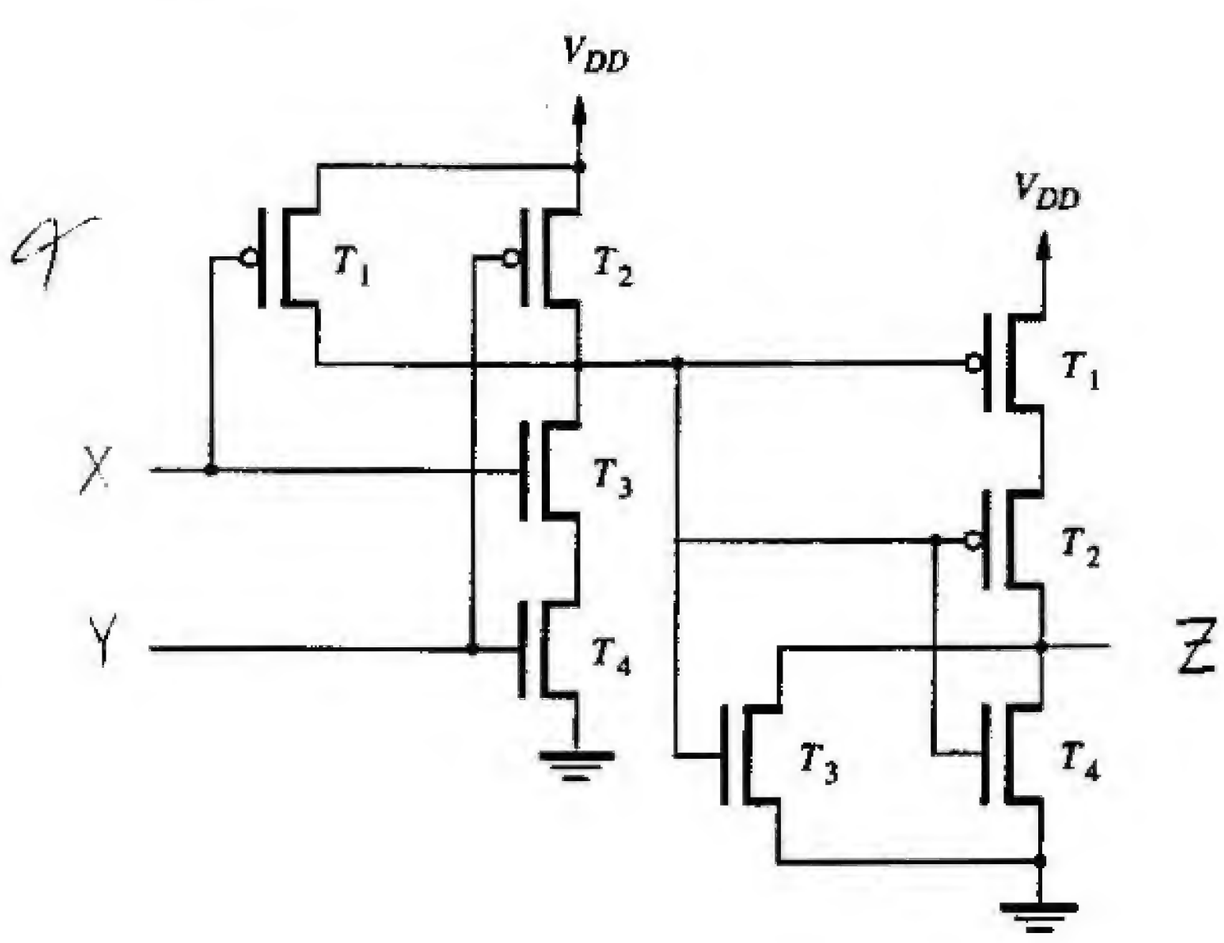
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY midterm IS
        PORT (      w1, w0, s      : IN    STD_LOGIC;
                    f              : OUT   STD_LOGIC);
END midterm;

ARCHITECTURE behavior OF midterm IS
BEGIN
        WITH s SELECT
            f <=    (w1 AND w0) WHEN '0'
                    (w1 OR w0) WHEN OTHERS;
END behavior;
```

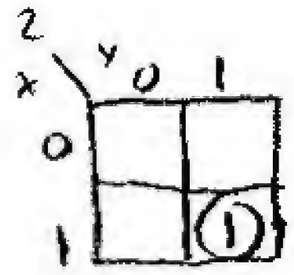


10. *(4 marks)* Express the logic function implemented by the following CMOS circuit in Sum Of Products form.



AND function

X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1



$Z = xy$

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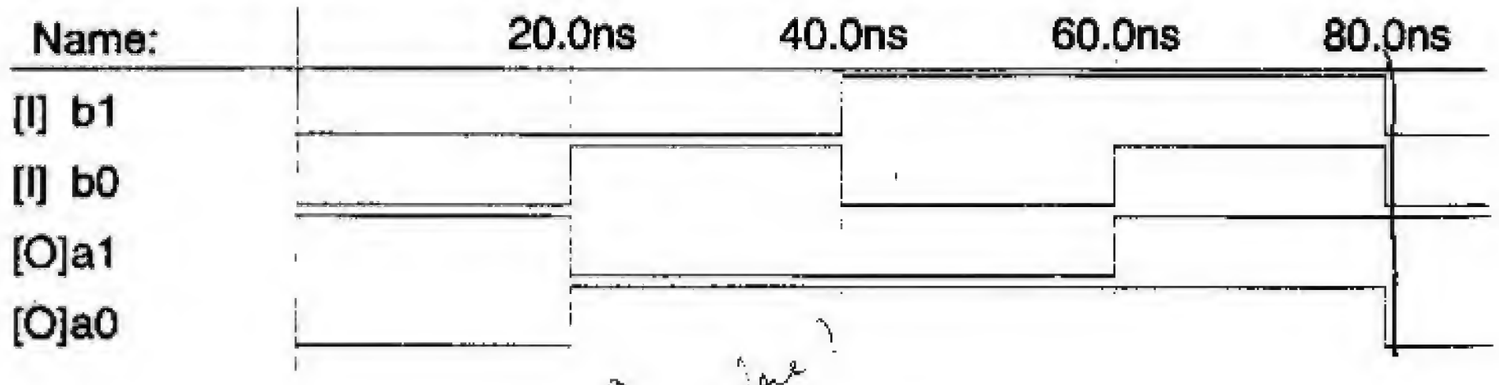
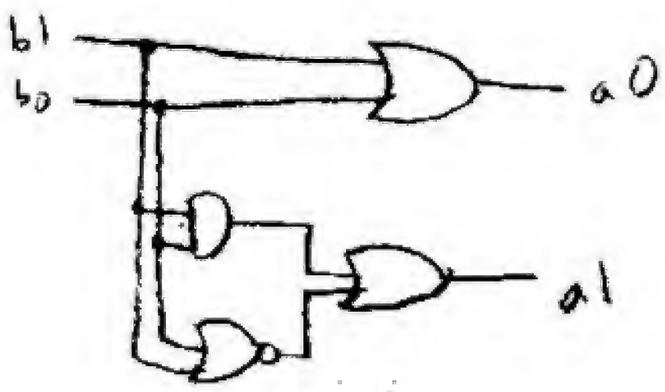
11. *(9 marks)* Analyze the following timing diagram to determine the logic function that it represents. Clearly state the logic function and design a circuit that implements the logic function using NAND gates only.

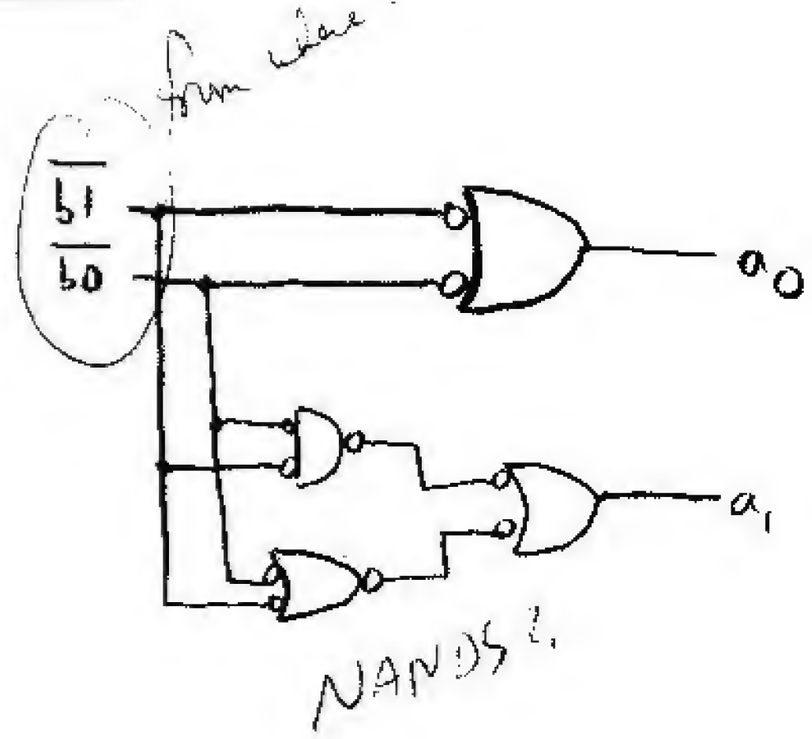


b_1	b_0	a_1	a_0
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	1

XNOR OR

a_1 = EXCLUSIVE NOR
a_0 = OR





(3)

12. *(6 marks)* What is *the* distinguishing characteristic for each of combinational, sequential, and synchronous systems.

A sequential system is a system where one thing is done and the next thing starts as soon as the first thing finishes.

(2) A combinational system is one where some parts can be done at the same time to speed up the system.

A synchronous system is where everything is done at the same time.